CLAIM AMENDMENTS

Please cancel claims 24-29 without prejudice or disclaimer.

Please amend claims 1-23 as follows.

Please add new claims 30-40.

1. (Currently Amended) A method, comprising:

allocating ~~an original~~ a first ~~percentage of~~ memory bandwidth ~~or number of accesses to memory by a memory controller~~; and

increasing the first memory bandwidth ~~or number of accesses allocated to the memory controller to a percentage higher than the~~ if a demand for memory bandwidth ~~original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller~~ is less than the first memory bandwidth ~~original percentage of bandwidth or number of accesses allocated to the memory controller~~; and

decreasing the first memory bandwidth ~~or number of accesses allocated to the memory controller to a percentage lower than~~ if a demand for memory bandwidth ~~an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are more~~ is greater than the first memory bandwidth ~~original percentage of bandwidth or number of accesses allocated to the memory controller~~.

2. (Currently Amended) The method of claim 1, further comprising:

setting a window of time to monitor the ~~percentage of~~ demand for memory bandwidth ~~or number of accesses to memory by the memory controller~~; and

measuring the ~~percentage of~~ demand for memory bandwidth ~~used or number of accesses to memory by the memory controller~~ during the window of time.

3. (Currently Amended) The method of claim 1, further comprising applying a mask to increase the memory bandwidth ~~or number of accesses allocated to the memory controller~~ to a ~~percentage higher than the~~ if a demand for memory bandwidth ~~original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory~~

~~controller~~ [[are]] is less than the first memory ~~original percentage of bandwidth or number of accesses allocated to the memory controller~~.

4. (Currently Amended) The method of claim 1, further comprising applying a mask to decrease the memory ~~bandwidth or number of accesses allocated to the memory controller~~ to a ~~percentage~~ value lower than the first value if a demand for memory bandwidth ~~an original bandwidth or number of accesses allocated when accesses to memory~~ by the memory controller [[are]] is less than the first value ~~original percentage of~~ bandwidth ~~or number of accesses allocated to the memory controller~~.

5. (Currently Amended) An article of manufacture article of manufacture, comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations comprising,

allocating ~~an original~~ a first ~~percentage of~~ memory bandwidth ~~or number of accesses to memory by a memory controller~~; and

increasing the first memory bandwidth ~~or number of accesses allocated to the memory controller to a percentage higher than the~~ if a demand for memory bandwidth ~~original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller~~ is less than the first memory bandwidth ~~original percentage of bandwidth or number of accesses allocated to the memory controller~~; and

decreasing the first memory bandwidth ~~or number of accesses allocated to the memory controller to a percentage lower than~~ if a demand for memory bandwidth ~~an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are more~~ is greater than the first memory bandwidth ~~original percentage of bandwidth or number of accesses allocated to the memory controller~~.

6. (Currently Amended) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising:

setting a window of time to monitor the ~~percentage of~~ demand for memory bandwidth ~~or number of accesses to memory by the memory controller~~; and

measuring the ~~percentage of~~ demand for memory bandwidth ~~used or number of accesses to memory by the memory controller~~ during the window of time.

7. (Currently Amended) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising applying a mask to increase the memory bandwidth ~~or number of accesses allocated to the memory controller~~ to a ~~percentage higher than the~~ if a demand for memory bandwidth ~~original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller~~ [[are]] is less than the first memory ~~original percentage of bandwidth or number of accesses allocated to the memory controller~~.

8. (Currently Amended) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising applying a mask to decrease the memory ~~bandwidth or number of accesses allocated to the memory controller~~ to a ~~percentage~~ value lower than the first value if a demand for memory bandwidth ~~an original bandwidth or number of accesses allocated when accesses to memory~~ by the memory controller [[are]] is less than the first value ~~original percentage of~~ bandwidth ~~or number of accesses allocated to the memory controller~~.

9. (Currently Amended) An apparatus, comprising:

~~a chipset having:~~

~~a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it; and~~

a memory controller to increase ~~the percentage of~~ a memory bandwidth ~~or the number of memory accesses allocated to the processor when the actual percentage of~~ if a demand for the memory bandwidth ~~or number of accesses to the memory by the processor~~ is less than a first memory ~~the original percentage of~~ bandwidth ~~or number of accesses allocated to the processor~~, the memory controller ~~further~~ to decrease the ~~percentage of~~ memory bandwidth ~~or the number of memory accesses allocated to the processor when the actual percentage of~~ if the demand for the memory bandwidth ~~or number~~

~~of memory accesses by the processor~~ is [[more]] greater than the first ~~original percentage of~~ memory bandwidth ~~or number of memory accesses allocated to the processor~~.

10. (Currently Amended) The apparatus of claim 9, further comprising:

a first register in the memory controller to set the ~~percentage of~~ memory bandwidth ~~or the number of memory accesses allocated to the processor~~;

a second register in the memory controller to set a window of time to monitor ~~percentage of~~ demand for memory bandwidth ~~or number of memory accesses used by the processor~~; and

a counter in the memory controller to measure ~~percentage of~~ demand for memory bandwidth ~~used or number of memory accesses by the processor~~ during the window of time.

11. (Currently Amended) The apparatus of claim 10, wherein the memory controller further comprises a mask to increase the ~~percentage of~~ memory bandwidth if ~~or the number of memory accesses allocated to the processor when~~ demand for memory bandwidth ~~accesses by the processor~~ is less than the first ~~percentage of~~ memory bandwidth ~~or the number of memory accesses allocated to the processor~~.

12. (Currently Amended) The apparatus of claim 10, wherein the memory controller further comprises a mask to decrease the ~~percentage of~~ memory bandwidth if demand for ~~or the number of memory accesses allocated to the processor when~~ memory bandwidth ~~accesses by the processor~~ is [[more]] greater than the first ~~percentage of~~ memory bandwidth ~~or the number of memory accesses allocated to the processor~~.

13. (Currently Amended) The apparatus of claim 9, further comprising ~~wherein the chipset further comprises~~:

~~a graphics memory having an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it; and~~

a graphics controller to increase ~~the percentage of~~ a graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the graphics memory~~

~~when the actual percentage of~~ if a demand for the graphics memory bandwidth ~~or number of graphics memory accesses~~ is less than a first ~~the original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to the graphics memory~~, the graphics controller ~~further~~ to decrease ~~the percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the graphics memory when the actual percentage of~~ if the demand for the graphics memory bandwidth ~~or number of graphics memory accesses~~ is greater [[more]] than the first ~~original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to the graphics memory~~.

14. (Currently Amended) The apparatus of claim 13, ~~wherein the chipset further comprises~~ further comprising one or more input/output (I/O) devices, an individual I/O device having ~~an original percentage of~~ a second graphics memory bandwidth ~~or number of graphics memory accesses allocated to it~~, the graphics controller to increase the ~~percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of~~ if a demand for the graphics memory bandwidth by the I/O device ~~or number of graphics memory accesses~~ is less than the ~~original percentage of~~ second graphics memory bandwidth ~~or number of graphics memory accesses allocated to the one or more I/O devices~~, the graphics controller ~~further~~ to decrease the ~~percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of~~ if a demand for the graphics memory bandwidth by the I/O device ~~or number of graphics memory accesses~~ is [[more]] greater than the ~~original percentage of~~ second graphics memory bandwidth ~~or number of graphics memory accesses allocated to the one or more I/O devices~~.

15. (Currently Amended) The apparatus of claim 13, further comprising a ~~wherein the~~ processor ~~further includes an original percentage of~~ having a second graphics memory bandwidth ~~or number of graphics memory accesses allocated to it~~, the graphics controller to increase the ~~percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses~~ if a demand for the graphics memory bandwidth by the processor is less than the second ~~original percentage of~~ graphics memory

bandwidth ~~or number of graphics memory accesses allocated to the processor~~, the graphics controller ~~further~~ to decrease the percentage of graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the processor when the actual percentage of~~ if a demand for the graphics memory bandwidth by the processor ~~or number of graphics memory accesses~~ is more than the second ~~original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to the processor~~.

16. (Currently Amended) The apparatus of claim 9, ~~wherein the chipset further comprises~~ further comprising a graphics memory having ~~an original percentage of~~ a first graphics memory bandwidth ~~or number of graphics memory accesses allocated to it~~, the graphics memory to increase ~~the percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to itself when an actual percentage of~~ if a demand for graphics memory bandwidth ~~or number of graphics memory accesses~~ is less than the first ~~the original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to itself~~, the graphics memory ~~further~~ to decrease the ~~percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to itself when the actual percentage of~~ if a demand for graphics memory bandwidth ~~or number of graphics memory accesses~~ is [[more]] greater than the first ~~original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to itself~~.

17. (Currently Amended) The apparatus of claim 16, further comprising ~~wherein the chipset further comprises~~ one or more input/output (I/O) devices, an individual I/O device having ~~an original percentage of~~ the first graphics memory bandwidth ~~or number of graphics memory accesses allocated to it~~, the graphics memory to increase ~~the percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of~~ if a demand for the graphics memory bandwidth by the I/O device ~~or number of graphics memory accesses~~ is less than the first ~~the original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to the one or more I/O devices~~, the graphics memory ~~further~~ to decrease the ~~percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of~~ if a demand for the graphics memory

bandwidth by the I/O device ~~or number of graphics memory accesses~~ is [[more]] greater than the first ~~original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to the one or more I/O devices~~.

18. (Currently Amended) The apparatus of claim 16, further comprising a ~~wherein the~~ processor having a second ~~further includes an original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to it~~, the graphics memory to increase the ~~percentage of~~ graphics memory bandwidth ~~or the number of graphics memory accesses allocated to the processor when an actual percentage of~~ if a demand for graphics memory bandwidth by the processor ~~or number of graphics memory accesses~~ is less than the second ~~original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to the processor~~, the graphics memory ~~further~~ to decrease the ~~percentage of~~ graphics memory bandwidth if a demand for ~~or the number of graphics memory accesses allocated to the processor when the actual percentage of~~ graphics memory bandwidth by the processor ~~or number of graphics memory accesses~~ is [[more]] greater than the second ~~original percentage of~~ graphics memory bandwidth ~~or number of graphics memory accesses allocated to the processor~~.

19. (Currently Amended) The apparatus of claim 9, ~~wherein the chipset further comprises~~ further comprising one or more input/output (I/O) devices having ~~an original percentage of~~ a first memory bandwidth ~~or number of memory accesses allocated to it~~, wherein the memory controller is to increase the ~~percentage of~~ memory bandwidth if a demand for the ~~or the number of memory accesses allocated to the one or more I/O devices when an actual percentage of~~ memory bandwidth ~~or number of memory accesses~~ by the one or more I/O devices is less than the first ~~the original percentage of~~ memory bandwidth ~~or number of memory accesses allocated to the one or more I/O devices~~, the memory controller ~~further~~ to decrease the ~~percentage of~~ memory bandwidth ~~or the number of memory accesses allocated to the one or more I/O devices when the actual percentage of~~ if a demand for the memory bandwidth ~~or number of memory accesses~~ by the one or more I/O devices is [[more]] greater than the first ~~original percentage of~~ memory bandwidth ~~or number of memory accesses allocated to the one or more I/O devices~~.

20. (Currently Amended) An apparatus, comprising:

a processor having ~~an original percentage of~~ a first memory bandwidth ~~or number of memory accesses allocated to it~~, the processor having further a memory controller to increase the ~~percentage of~~ first memory bandwidth ~~or the number of memory accesses allocated to the processor when the actual percentage of~~ if a demand for the memory bandwidth ~~or number of accesses to the memory~~ by the processor is less than the first memory bandwidth ~~the original percentage of bandwidth or number of accesses allocated to the processor~~, the memory controller ~~further~~ to decrease the ~~percentage of~~ first memory bandwidth ~~or the number of memory accesses allocated to the processor when the actual percentage of~~ if a demand for memory bandwidth ~~or number of memory accesses~~ by the processor is [[more]] greater than the first ~~original percentage of~~ memory bandwidth ~~or number of memory accesses allocated to the processor~~.

21. (Currently Amended) The apparatus of claim 20, further comprising:

a first register in the memory controller to set the ~~percentage of~~ memory bandwidth ~~or the number of memory accesses allocated to the processor~~;

a second register in the memory controller to set a window of time to monitor ~~percentage of~~ demand for memory bandwidth ~~or number of memory accesses used by the processor~~; and

a counter in the memory controller to measure ~~percentage of~~ demand for memory bandwidth ~~used or number of memory accesses by the processor~~ during the window of time.

22. (Currently Amended) The apparatus of claim 20, wherein the memory controller further comprises a mask to increase the ~~percentage of~~ memory bandwidth if ~~or the number of memory accesses allocated to the processor when~~ demand for memory bandwidth ~~accesses by the processor~~ is less than the first ~~percentage of~~ memory bandwidth ~~or the number of memory accesses allocated to the processor~~.

23. (Currently Amended) The apparatus of claim 20, wherein the memory controller further comprises a mask to decrease the ~~percentage of~~ memory bandwidth if demand for ~~or the number of memory accesses allocated to the processor when~~ memory bandwidth ~~accesses by the processor~~ is [[more]] greater than the first ~~percentage of~~ memory bandwidth ~~or the number of memory accesses allocated to the processor~~.

Claims 24-29. (Canceled).

30. (New) A system, comprising:

a direct random access memory; and

a memory controller to increase a memory bandwidth if a demand for the memory bandwidth is less than a first memory bandwidth, the memory controller to decrease the memory bandwidth if the demand for the memory bandwidth is greater than the first memory bandwidth.

31. (New) The system of claim 30, further comprising:

a first register in the memory controller to set the memory bandwidth;

a second register in the memory controller to set a window of time to monitor demand for memory bandwidth; and

a counter in the memory controller to measure demand for memory bandwidth during the window of time.

32. (New) The apparatus of claim 31, wherein the memory controller further comprises a mask to increase the memory bandwidth if demand for memory bandwidth is less than the first memory bandwidth.

33. (New) The system of claim 31, wherein the memory controller further comprises a mask to decrease the memory bandwidth if demand for memory bandwidth is greater than the first memory bandwidth.

34. (New) The system of claim 30, further comprising:

a graphics controller to increase a graphics memory bandwidth if a demand for the graphics memory bandwidth is less than a first graphics memory bandwidth, the graphics controller to decrease graphics memory bandwidth if the demand for the graphics memory bandwidth is greater than the first graphics memory bandwidth.

35. (New) The system of claim 34, further comprising one or more input/output (I/O) devices, an individual I/O device having a second graphics memory bandwidth, the graphics controller to increase the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is less than the second graphics memory bandwidth, the graphics controller to decrease the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is greater than the second graphics memory bandwidth.

36. (New) The system of claim 34, further comprising a processor having a second graphics memory bandwidth, the graphics controller to increase the graphics memory bandwidth if a demand for the graphics memory bandwidth by the processor is less than the second graphics memory bandwidth ~~or~~, the graphics controller to decrease the percentage of graphics memory bandwidth if a demand for the graphics memory bandwidth by the processor is more than the second graphics memory bandwidth.

37. (New) The system of claim 30, further comprising a graphics memory having a first graphics memory bandwidth, the graphics memory to increase graphics memory bandwidth if a demand for graphics memory bandwidth is less than the first graphics memory bandwidth, the graphics memory to decrease the graphics memory bandwidth if a demand for graphics memory bandwidth is greater than the first graphics memory bandwidth.

38. (New) The system of claim 37, further comprising one or more input/output (I/O) devices, an individual I/O device having the first graphics memory bandwidth, the graphics memory to increase graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is less than the first graphics memory bandwidth, the graphics

memory to decrease the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is greater than the first graphics memory bandwidth.

39. (New) The system of claim 37, further comprising a processor having a second graphics memory bandwidth, the graphics memory to increase the graphics memory bandwidth if a demand for graphics memory bandwidth by the processor is less than the second graphics memory bandwidth, the graphics memory to decrease the graphics memory bandwidth if a demand for graphics memory bandwidth by the processor is greater than the second graphics memory bandwidth.

40. (New) The system of claim 30, further comprising one or more input/output (I/O) devices having a first memory bandwidth, wherein the memory controller is to increase the memory bandwidth if a demand for the memory bandwidth by the one or more I/O devices is less than the first memory bandwidth, the memory controller to decrease the memory bandwidth if a demand for the memory bandwidth by the one or more I/O devices is greater than the first memory bandwidth.

41. (New) A system, comprising:

a direct random access memory; and

a processor having a first memory bandwidth, the processor having further a memory controller to increase the first memory bandwidth if a demand for the memory bandwidth by the processor is less than the first memory bandwidth, the memory controller to decrease the first memory bandwidth if a demand for memory bandwidth by the processor is greater than the first memory bandwidth.

42. (New) The system of claim 41, further comprising:

a first register in the memory controller to set the memory bandwidth;

a second register in the memory controller to set a window of time to monitor demand for memory bandwidth; and

a counter in the memory controller to measure demand for memory bandwidth during the window of time.

43. (New) The system of claim 41, wherein the memory controller further comprises a mask to increase the memory bandwidth if demand for memory bandwidth is less than the first memory bandwidth.

44. (New) The system of claim 41, wherein the memory controller further comprises a mask to decrease the memory bandwidth if demand for memory bandwidth is greater than the first memory bandwidth.